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# An Interleaved Boost Converter with LC Coupled Soft Switching

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**ABSTRACT**

A novel soft switching technique for interleaved boost converter with ZVS and ZCS during ON and OFF conditions of the main switches, it can operated in duty cycle (D) is greater than 0.5 and less than 0.5 proposed in this paper. By using the interleaved approach this network topology not only decreases the current stress on the main circuit model also decay the ripple of the input current and output voltage. Here by establishing the common soft switching device, this soft switching interleaved converter can highly reduce the size and cost. This model has faster switching and accurate impedance adjustability is achieved with the decay of the auxiliary circuit reactance, then it contributed much increase the overall performance. And this technique can be reduces the switching losses and improve the efficiency by ZVS technique, but it does not improve the turn-off switching losses by a ZCS technique. The entire ripple and Total harmonic distortions can be reduced in this technique; there are no changes on performance and the converter efficiency. A model simulation is designed using the "MATLAB Simulink" gives the good results of the proposed converter.

**Keywords:** Interleaved Boost Converter, Soft Switching, Zero Voltage Switching (ZVS), Zero Current Switching (ZCS).

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## 1. INTRODUCTION

The Boost converter techniques are popular way for most power electronic systems to serve a pre-regulator, due to advantage of simplicity and higher performance. An interleaved topology improves converter performance at the cost of additional inductor, power switching devices, and output rectifiers. This interleaving can be reducing the output capacitor ripple current as a function of duty cycle. As the duty cycle approaches 0%, 50%, and 100% duty cycle, the sum of the two diode currents approaches dc. At these points the output capacitor only has to filter the inductor ripple current. These conventional boost converters are not suitable for the practical device that produces low voltage levels, requiring large set up voltage and also obtain such high gain.

This paper proposes a novel interleaved boost converter with both characteristics of Zero-Voltage turn-ON and Zero-Current turn-OFF for the main switches to improve the efficiency with a wide range of load. The voltage stresses of the main switches and auxiliary switch are equal to the output voltage and the duty cycle of the proposed topology can be increased to more than 50%. The proposed converter is the parallel of two boost converters and their driving signals stagger $180^{o}$ this makes the operation assumed symmetrical. It uses the interleaved boost topology and applies the common soft-switching circuit. The Resonant circuit consists of the resonant inductor $L_r$, resonant capacitor $C_r$ parasitic capacitors $C_{sa}$, $C_{sb}$ and auxiliary switch $S_r$ to become a resonant way to reach ZVS and ZCS functions.

The interleaved boost converters with ZCS or ZVS are proposed. These topologies have higher efficiency than the conventional boost converter because the proposed circuits have decreased the switching losses of the main switches with ZCS or ZVS. Nevertheless, these circuits can just achieve the junction of ZVS or ZCS singly or need more auxiliary circuits to reach the soft switching. In, the soft-switching circuit for the interleaved boost converter is proposed. However, its main switches are zero-current turn-ON and zero-voltage turn-OFF and the converter works in the discontinuous mode. It does not reduce the switching losses of the interleaved boost converter by the soft-switching techniques.

## 2. RELATED WORK

This study a soft-switching technique for interleaved boost converter composed of two shunted elementary boost conversion units and an auxiliary inductor. The converter is able to turn on both the active power switches at zero voltage to reduce their switching losses and evidently improve the conversion efficiency. Since the two parallel-operated elementary boost units are identical, operation analysis and design for the converter module becomes quite simple. A laboratory test circuit is built, and

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the circuit operation shows satisfactory agreement with the theoretical analysis. The experimental results show that this converter module performs very well with the output efficiency as high as 95%.

**3. DESIGN AND ANALYSIS**

The design of circuit is analyzed in Continuous Conduction Mode CCM with different load ranges having different duty cycles. The research interleaved boost converter with LC coupled soft switching is shown in Fig.3.1. It can be utilizes the interleaved boost converter topology and applies enhanced soft switching methodology where the resonant tank itself triggers the switches for extreme condition. This resonant tank is composed of resonant capacitor $C_{rc}$ and resonant inductor $L_{rc}$ which in turn act as a control circuit for the auxiliary switch $S_{ax}$, that is responsible for ZVS and ZCS function.

The design model is operated in fundamental mode with duty cycle D which is exact symmetrical in function. The circuit is analyses with certain assumptions to simplify the current analysis which are listed as

- All electronic switches and diodes are assumed to be in practical condition with an exponential decay in the computation for theoretical analysis.
- Idealizing the input and output reactance.
- The two boost inductors are coupled.
- Same duty cycles (D1=D2) for the main switches $S_{s1}$ and $S_{s2}$.

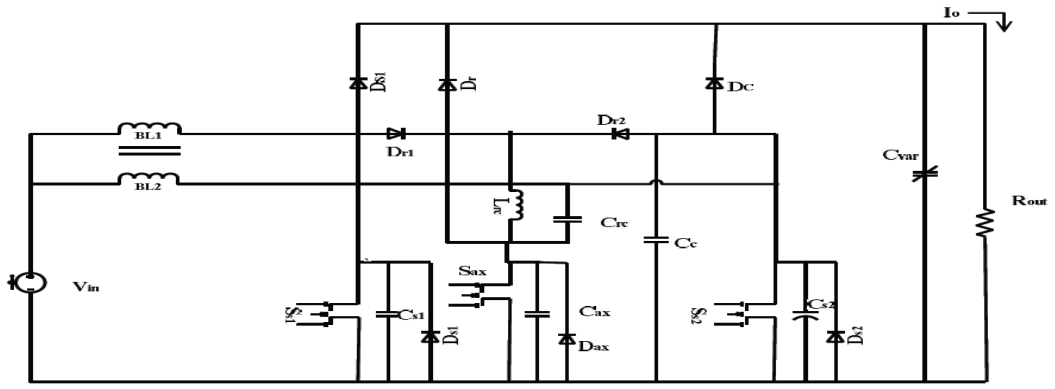


**Fig.3.1.1** proposed LC Resonant tank interleaved Boost Converter.

The flow of current in initial phases through the boost inductor has an effect of interference which results in addition of ripples. Thus for the initial input current to be clear from input ripple, a guard is introduced which magnetic couple by a ferrite core which has high permittivity and hence the coupling is more effective.

Boost inductors $B_{L1}$ and $B_{L2}$ is energized by the magnetic flow across the inductor causing fluctuation in the input current. It is minimized by placing the iron core between the coils which looks like a transformer arrangement. Thus the flow of current us regulated by the magnetic coupling across the inductors.

The mutual inductance of exerted by both the boost inductor is given by

$$L_m = (\mu_r \sqrt{L_1 L_2})\, K \qquad (1)$$

Where $\mu_r$ &K are permittivity of the core and coupling co-efficient respectively.

According to the circuit theory, the coupled inductor can be realized with an uncoupled inductor which needs an additional inductor for coupling.

$$L_1' = L_1 - L_m \qquad (2)$$

$$L_2' = L_2 - L_m \qquad (3)$$

Here $L_1'$&$L_2'$ are considered to be a leakage inductances which has major influence over the input current ripple. By regulating the coupling coefficient, the amount of ripples in the input current can be controlled. On the other hand the output from the inductor is given by the expression which depends only on the leakage inductance.

$$\frac{di_{L1}}{dt} = \frac{v_o}{L_1' + L_m} = \frac{v_o}{L_1} \qquad (4)$$

$$\frac{di_{L2}}{dt} = \frac{v_o}{L_2' + L_m} \qquad (5)$$

It is an inevitable fact that, in practical conditions, it is not possible to produce the duty cycle exactly at 50%., hence the design is analyzed in duty cycle (D) less than 50%.

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### 3.1 OPERATIONAL ANALYSIS

Amidst 16 operational nodes in one complete cycle, only 8 nodes related with main switch $S_{s1}$ are analysed and corresponding analytical equations are derives. The operating modes of the circuit for duty cycle less than 50%. The initial voltage applied to the switch tends to vary due to the magnetic coupling in the inductor. Now the diodes $D_{r1}$, $D_{s1}$ becomes active, which act as a rectifier diode. The clamped diode $D_r$ is turned off by the positive input cycle. At this junction controls of switched are excited by pulse which is meant to turn off the switch $S_{s1}$, $S_{s2}$. Hence the parasitic capacitance $C_{s1}$, $C_{s2}$ attached with the main switched and coupling capacitance share equal voltage. So it is given that $V_{c1}=V_{c2}= V_{cc} =V_0$ as the closed loop have equal voltage. At the end time the resonant inductor share the voltage applied across the circuit and the rectifier diode gets turned off. It uses the interleaved boost topology and applies the common soft-switching circuit. The resonant circuit consists of the resonant inductor $L_r$ resonant capacitor $C_r$ parasitic capacitors $C_{sa}$, $C_{sb}$ and auxiliary switch $S_r$ to become a resonant way to reach ZVS and ZCS functions. Fig.3.1.1 shows the two operating modes of this circuit, depending on whether the duty cycle of the main switch is more than 50% or not.

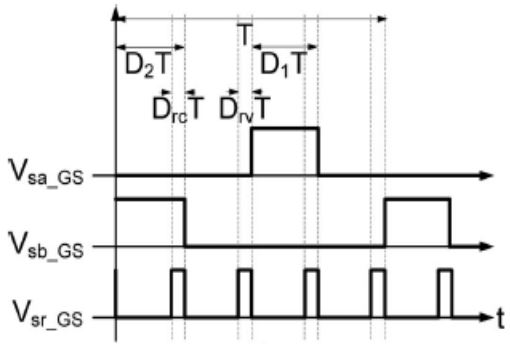


Fig. 3.1.1(a) switching based on D < 0.5.

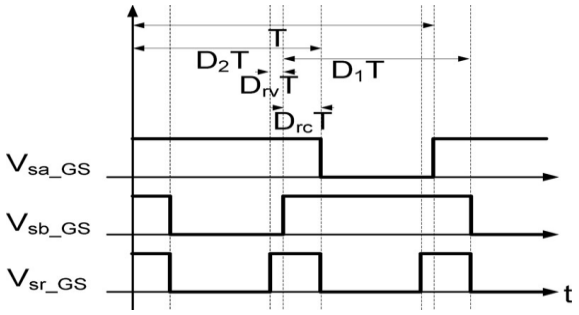


Fig. 3.1.1(b) switching based on D > 0.5

### 3.2 Operational Analysis of D < 50% Mode

The operating principle of the proposed topology is described in this section. There are 24 operational modes in the complete cycle. Only the 12 modes related to the main switch $S_a$ are analyzed, because the interleaved topology is symmetrical. Fig.3.3 shows the related waveforms when the duty cycle of the main switch is less than 50%. There are some assumptions to simplify the circuit analysis.

1) All power switches and diodes are ideal.

2) The input inductor and output capacitor are ideal.

3) The two inductors are equal; Boost_$L_1$ = Boost_$L_2$

4) The duty cycles of the main switches are equal; $D_1 = D_2$

During **Stage1**, as shown in Fig.3.2.1 the main switches $S_a$ and $S_b$ are turned OFF, the auxiliary switch $S_r$ and the rectifier diodes $D_a$ and $D_b$ are turned ON, and the clamped diode $D_r$ is turned OFF. The voltages across the parasitic capacitors $C_{sa}$ and $C_{sb}$ of the main switches and the resonant capacitor $C_r$ are all equal to the output voltage; i.e., $V_{sa} = V_{sb} = V_{sr} = V_o$ in the previous mode. The resonant inductor current $I_{Lr}$ linearly ramps up until it reaches $I_{in}$ at t=t1 . When the resonant inductor current $I_{Lr}$ is equal to $I_{in}$ the Stage 1 will end. Then, the rectifier diodes are turned OFF.

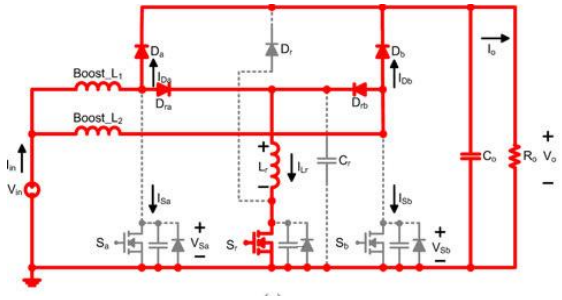


Fig.3.2.1 mode1.

In **Stage2**, the resonant inductor current continues to increase to the peak value, and the main switch voltages $V_{Sa}$ and $V_{Sb}$ decrease to zero, because the resonance occurs among $C_{Sa}$, $C_{Sb}$, $C_r$ and $L_r$. Then, the body diodes $D_{Sa}$ ($S_a$ ) and $D_{Sb}$ ($S_b$ ) can be turned ON.

In **Stage3** the end of mode 2, the main switch voltage $V_{sa}$ decreases to zero, so the body diode $D_{sa}$ of *Sa* is turned ON at $t_2$. At this time, the main switch can achieve ZVS. The on-time $t_3$ of the auxiliary switch $S_r$ needs to be more than $t_{01} + t_{12}$ to achieve the function of ZVS.

In **Stage4** the auxiliary switch $S_r$ is turned OFF and the clamped diode $D_r$ is turned ON. During this interval, the energy

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stored in the resonant inductor $L_r$ is transferred to the output load. The resonant inductor current $I_{lr}$ decreases to zero and the clamped diode $D_r$ is turned OFF at $t_4$.

In this **Stage5** the clamped diode $D_r$ is turned OFF. The energy of the boost_$L_2$ is transferred to $C_r$ and $C_{sb}$ and the energy stored in the parasitic capacitor $C_{sr}$ of the auxiliary switch is transferred to the resonant inductor $L_r$ and resonant capacitor $C_r$ at this time. The rectifier diode $D_b$ is turned ON when the voltage across the main switch $S_b$ reaches $V_o$ at $t=t_5$.

In **Stage6 t**he parasitic capacitor $C_{Sr}$ of the auxiliary switch is linearly charged by $I_{L2}-I_o$ to $V_o$. Then, the clamped diode *Dr* is turned ON at $t_6$.

In **Stage7** the clamped diode $D_r$ is turned ON. The energy stored in the resonant inductor $L_r$ is transferred to the output load by the clamped diode $D_r$. At $t_7$, the clamped diode $D_r$ is turned OFF because the auxiliary

Switch $S_r$ is turned ON.

In **Stage8** the resonant inductor current $I_{Lr}$ increases linearly until it reaches $I_{L2}$ and the rectifier diode current $I_{Db}$ decreases to zero at $t = t_a$, so the rectifier diode $D_b$ is turned OFF.

In **Stage9** the resonant inductor current $I_{Lr}$ is equivalent to a constant current source. In order to meet the demand that the main switch $S_a$ is turned OFF under the ZCS condition, $i_{Lr} \approx i_{Lr}$ must be greater than $I_{in}$. Then the main switch currents $I_{Sa}$ and $I_{Sb}$ are less than or equal to zero, so the main switch $S_a$ is turned OFF under the ZCS condition.

In **Stage10** when the main switch Sa and the auxiliary switch $S_r$ are turned OFF, the energy stored in the resonant inductor $L_r$ is transferred to the output load by the clamped diode $D_r$. When the resonant inductor current $I_{Lr}$ decreases to zero at $t_{10}$, the clamped diode $D_r$ is turned OFF. Then, the capacitors $C_{Sa}$, $C_{Sb}$, and $C_r$ are charged by $I_{in}$.

In **Stage11 t**he capacitors $C_{Sa}$, $C_{Sb}$, and $C_r$ are linearly charged by $I_{in}$ to $V_o$ , and the rectifier diodes $D_a$ and $D_b$ are turned ON at $t_{11}$.

In **Stage12** the operation of the interleaved boost topology is identical to that of the conventional boost converter. The ending time $t_{12}$ is equal to the starting time $t_0$ of another cycle, because the operation of the interleaved topology is symmetrical.

The waveforms presenting the operational mode of D < 0.5 is shown in Fig.3.3.1.

**3.3 Operational Analysis of D > 50% Mode**

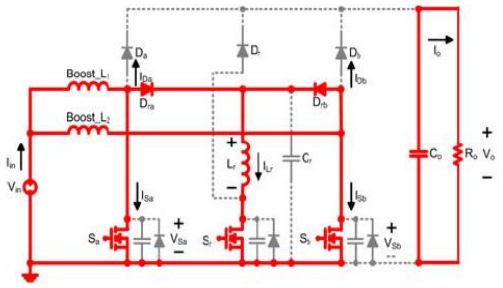


Fig.3.3.1 The operational analysis of D>0.5 stage1.

In **Stage1** as shown in **Fig.3.3,** all switches $S_a$ , $S_b$ , and $S_r$ are turned ON, and the rectifier diodes $D_a$ and $D_b$ and clamped diode $D_r$ are turned OFF. The main switch currents $I_{Sa}$ and $I_{Sb}$ are less than or equal to zero when the previous mode ends. The main switch $S_b$ can achieve the ZCS characteristic at $t = t_1$.

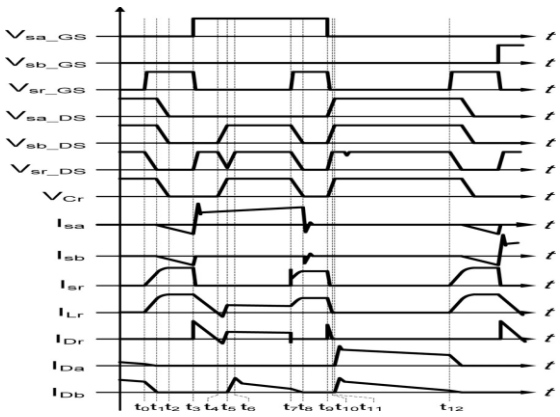


Fig. 3.3.1 waveforms of the designed converter.

In **Stage2** the energy stored in the resonant inductor $L_r$ is transferred to the output load by the clamped diode $D_r$, because the auxiliary switch $S_r$ is turned OFF. When the resonant inductor current $I_{Lr}$ decreases linearly until it reaches zero at $t = t_2$, the clamped diode $D_r$ is turned OFF.

In **Stage3** the clamped diode $D_r$ is turned OFF. The energy stored in the boost_L2 and the energy stored in the parasitic capacitor $C_{Sr}$ of the auxiliary switch are transferred to the resonant inductor $L_r$, resonant capacitor Cr, and parasitic capacitor $C_{Sb}$ of the main switch at this time. The rectifier diode $D_b$ is turned ON when the main switch voltage $V_{Sb}$ and resonant capacitor voltage $V_{Cr}$ increase to $V_o$ at $t = t_3$ .

In **Stage4** the parasitic capacitor $C_{Sr}$ of the auxiliary switch is linearly charged by $I_{L2} - I_o$ to $V_o$. Then, the clamped diode $D_r$ is turned ON at $t_4$.

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In **Stage5** the clamped diode $D_r$ is turned ON. The energy stored in the inductor $L_r$ is transferred to the output load by the clamped diode Dr. The clamped diode $D_r$ is turned OFF when the auxiliary switch $S_r$ is turned ON at t = t5.

In **Stage6** the interval, the resonant inductor current $I_{Lr}$ increases linearly until it reaches $I_{L2}$ and the rectifier diode current $I_{Db}$ decreases to zero at $t = t_a$, then the rectifier diode $D_b$ is turned OFF.

In **Stage7** when the resonant capacitor voltage $V_{Cr}$ and the main switch voltage $V_{Sb}$ are equal to zero, the body diode $D_{Sb}$ of $S_b$ is turned ON. Then, Mode 7 will start. In this mode, the resonant inductor current ILr is equal to a constant current source. If the condition of $i_{Lr}(t_6) \approx i_{Lr}(t_7) \geq I_{in}$ can be satisfied, the main switch currents $I_{Sa}$ and $I_{Sb}$ can be less than or equal to zero. Then, the main switch $S_a$ can be turned OFF under the ZCS condition. And the main switch $S_b$ reaches ZVS because of the conduction of the body diode $D_{Sb}$ in this mode.

The waveforms of the converter for D > 0.5 is shown in **Fig.3.3.2.** The interleaved boost converter operating in the continuous conduction mode (CCM) with both ZVS and ZCS characteristics.

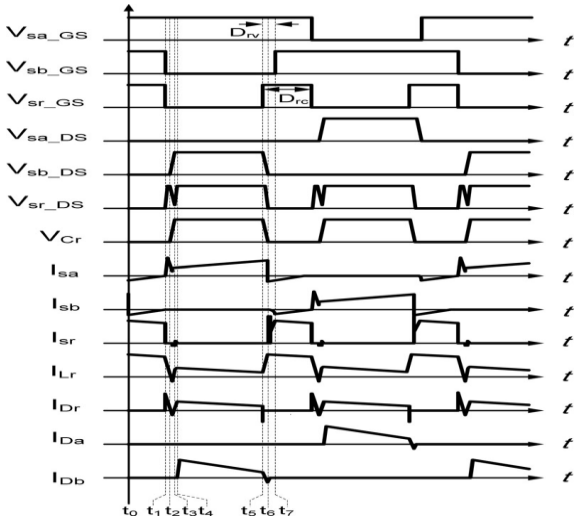


Fig.3.3.2 waveforms of the designed converter for D > 0.5.

## 4. SIMULATION RESULTS

### 4.1 OPEN LOOP SYSTEM

The open loop system is implemented in MATLAB SIMULINK. As per the converter the two simulations are considered. One operation of the converter is when the duty cycle (D) is maintained less than 0.5. and greater than 0.5. Simulated results are plotted.

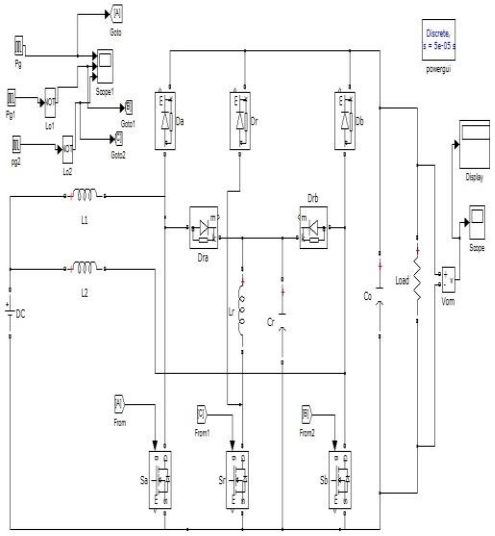

**Fig.4.1. 1 Simulation of the open loop system of the converter [ D<0.5 ] in MATLAB**

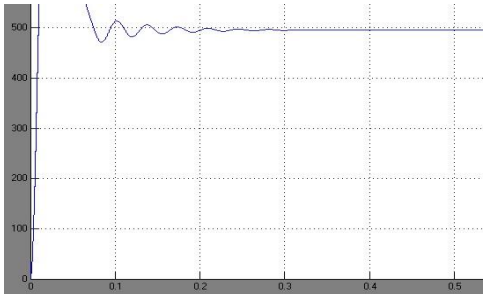


**Fig.4.1.2. Output voltage waveform**

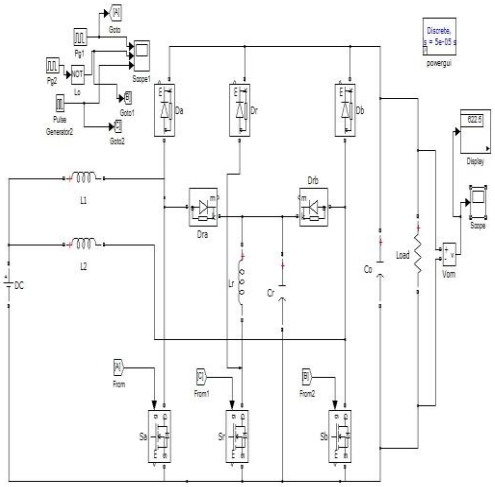

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**Fig.4.1.3. Simulation of the open loop system of the converter [ D>0.5 ] in MATLAB**

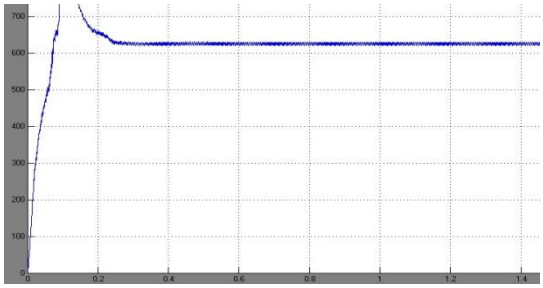

**Fig.4.1.4. Output voltage waveform**

### 1.1. CLOSED LOOP SYSTEM

The closed loop system is implemented in MATLAB SIMULINK. For closed loop simulation using PI controller, stage of D>0.5 are considered. Simulated results are presented.

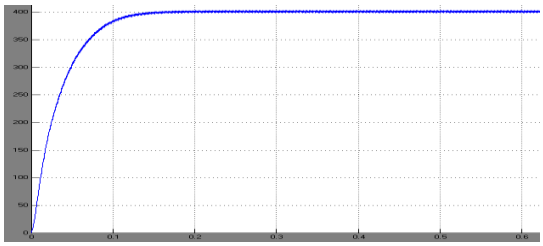

**Fig.4.6. Output voltage waveform**

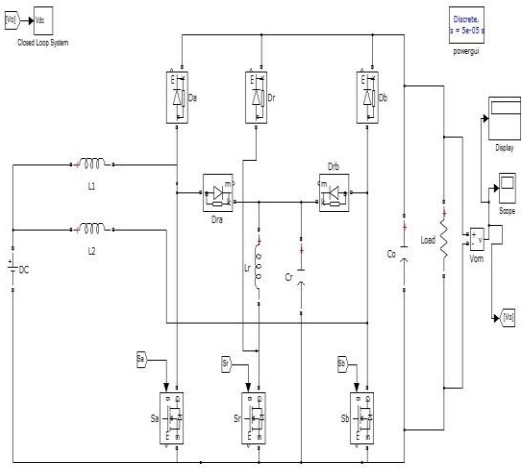

**Fig.4.1.5. Simulation of the closed loop system of the converter [ D>0.5 ] in MATLAB**

**4.2 SIMULATION DESIGN ZERO VOLTAGE SWITCHING OVERVIEW**

Zero voltage switching can best be defined as conventional square wave power conversion during the switch's on-time with "resonant" switching transitions. For the most part, it can be considered as square wave power utilizing a constant off-time control which varies the conversion frequency, or on-time to maintain regulation of the output voltage. For a given unit of time, this method is similar to fixed frequency conversion which uses an adjustable duty cycle. Regulation of the output voltage is accomplished by adjusting the effective duty cycle, performed by varying the conversion frequency. This changes the effective on-time in a ZVS design. The foundation of this conversion is simply the volt-second product equating of the input and output. It is virtually identical to that of square wave power conversion, and vastly unlike the energy transfer system of its electrical dual, the zero current switched converters.

During the ZVS switch off-time, the L-C tank circuit resonates. This traverses the voltage across the switch from zero to its peak, and back down again to zero. At this point the switch can be reactivated, and lossless zero voltage switching facilitated. Since the output capacitance of the MOSFET switch (Co& has been discharged by the resonant tank, it does not contribute to power loss or dissipation in the switch. Therefore, the MOSFET transition losses go to zero - regardless of operating frequency and input voltage. This could represent a significant savings in power, and result in a substantial improvement in efficiency. Obviously, this attribute makes zero voltage switching a suitable candidate for high frequency, high voltage converter designs. Additionally, the gate drive requirements are somewhat reduced in a ZVS design due to the lack of the gate to drain (Miller) charge, which is deleted when $\mathbf{V_{ds}}$ equals zero. The technique of zero voltage switching is applicable to all switching topologies; the buck regulator and its derivatives (forward, half and full bridge), the flyback, and boost converters, to name a few.

In the open loop system design in SIMULINK, the simulation of D<0.5, the input voltage of 250V is converted in to 500V, and for D>0.5, the input voltage of 150V is converted in to 623V.

In the closed loop system design in SIMULINK, the simulation of 150V is converted in to 400V for the design of D > 0.5 using PI controllers for the values of $k_p$=1; $k_i$=1.

**5. CONCLUSION**

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Improved soft switching technique for an interleaved boost converter operating under less than 50% duty cycle and grater then 50% duty cycle is proposed in this paper. The main switches $S_{s1}$ and $S_{s2}$ can also be adjusted by driving circuit through the LC resonant. The sharing of input current is equal between the switches. The circuit can be drive heavy load with greater efficiency due to impedance matching which is achieved by energy storing elements ( resonant tank and variable output capacitor ). This project is implemented in MATLAB SIMULINK and the results are presented. And its input voltage is form 150 to 250 and output voltage is 400v.

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